What is claimed is:

1. An apparatus for sampling timing compensation at a receiver of a communication system, wherein each of a first symbol and a second symbol comprising at least two pilot signals transmitted via a first and a second pilot subchannels respectively, and the first and the second pilot subchannels comprise a first and a second pilot indexes respectively, the apparatus comprising:

   a pilot subchannel estimator for generating a frequency response of the first and the second symbols according to the pilot signals of the first and the second symbols respectively;

   a timing offset estimator, coupled to the pilot subchannel estimator, for calculating a timing offset according to a sampling frequency offset, wherein the sampling frequency offset is generated according to the frequency responses of the first and the second symbols; and

   a phase rotator, coupled to the timing offset estimator, for performing sampling timing compensation according to an phase rotation corresponding to the timing offset.

2. The apparatus of claim 1, wherein the communication system is a multi-carrier system.

3. The apparatus of claim 1, wherein the timing offset estimator further comprises a phase difference calculating device for calculating a phase difference between the frequency responses of both the first and the second symbols, and a divider for calculating a timing offset through dividing the phase difference by a difference of the first and the second pilot indexes.

4. The apparatus of claim 3, wherein when the symbol comprises more than two pilot signals transmitted via more than two subchannels, the timing offset estimator further comprises a phase difference calculating device for calculating at least two phase differences between the frequency responses of at least two pairs of the symbols respectively; a divider for dividing each of the phase differences by a difference of the pilot indexes

of the subchannels transmitting the corresponding symbols; and an timing offset calculating device for calculating the timing offset through averaging the dividing results.

5. The apparatus of claim 1, further comprises:

a timing controller for generating a control signal according to the timing offset; and

a cyclic prefix remover for removing a cyclic prefix of the symbol according to the control signal.

6. The apparatus of claim 1, further comprising:

a timing controller for generating a control signal according to the timing offset;

a clock generator for generating a sampling clock according to the control signal, wherein the phase of the sampling clock is adjusted according to the control signal; and

an analog-to-digital converter (ADC) for converting the symbol according to the sampling clock.

7. The apparatus of claim 6, wherein period of the sampling clock (Tf) is shorter than the sampling interval (Ts) of the ADC.

8. The apparatus of claim 7, wherein period of the sampling clock (T_f) is a fraction of the sampling interval (T_s) of the ADC.

9. The apparatus of claim 6, wherein the clock generator further comprises a phase-locked loop (PLL) circuit.

10. A method for sampling timing compensation used at a receiver of a communication system, wherein each of a first symbol and a second symbol comprising at least two pilot signals transmitted via a first and a second pilot subchannels respectively, and the first and the second pilot subchannels comprise a first and a second pilot indexes respectively, comprising:

generating a frequency response of the first and the second symbol according to the pilot signals of the first and the second symbols

respectively;

generating a sampling frequency offset according to the frequency responses of the first and the second symbols;

calculating a timing offset according to the sampling frequency offset; and

performing sampling timing compensation according to a phase rotation corresponding to the timing offset.

11. The method of claim 10, wherein the sampling frequency offset is generated through calculating a phase difference between the frequency responses of both the first and the second symbols.

12. The method of claim 11, wherein the timing offset is calculated through dividing the phase difference by a difference of the first and the second pilot indexes.

13. The method of claim 10, wherein when the symbol comprises more than two pilot signals transmitted via more than two subchannels, the sampling frequency offset is generated through calculating at least two phase differences between the frequency responses of at least two pairs of the symbols respectively.

14. The method of claim 13, wherein the timing offset is calculated through dividing each of the phase differences by a difference of the pilot indexes of the subchannels transmitting the corresponding symbols, and calculating the timing offset through averaging the dividing results.

15. The method of claim 10, further comprising:

generating a control signal according to the timing offset; and

removing a cyclic prefix of the symbol according to the control signal.

16. The method of claim 10, further comprising:

generating a control signal according to the timing offset;

generating a sampling clock according to the control signal, wherein the phase of the sampling clock is adjusted according to the control signal; and

converting the symbol according to the sampling clock.

17. The method of claim 13, wherein period of the sampling clock (T_f) is a fraction of the sampling interval (T_s) of the ADC.

18. An apparatus for sampling timing compensation at a receiver of a communication system, wherein each of a first symbol and a second symbol comprising at least two pilot signals transmitted via a first and a second pilot subchannels respectively, and the first and the second pilot subchannels comprise a first and a second pilot indexes respectively, the apparatus comprising:

a pre-FFT processing device for processing the first and the second symbols in a time domain;

a FFT for transforming the first and the second symbols to a frequency domain;

a pilot subchannel estimator for generating a frequency response of the first and the second symbols according to the pilot signals of the first and the second symbols respectively;

a timing offset estimator, coupled to the pilot subchannel estimator, for calculating a timing offset according to a sampling frequency offset, wherein the sampling frequency offset is generated according to the frequency responses of the first and the second symbols;

a phase rotator, coupled to the timing offset estimator, for performing sampling timing compensation according to an phase rotation corresponding to the timing offset; and

a adjusting device for adjusting the operation of the pre-FFT processing device.

19. The apparatus of claim 18, wherein the pre-FFT processing device includes an ADC.

20. The apparatus of claim 19, wherein the adjusting device includes:

a timing controller for generating a control signal according to the timing offset; and

a clock generator for generating a sampling clock according to the control signal for controlling the operation of the ADC, wherein the phase of the sampling clock is adjusted according to the control signal.

21. The apparatus of claim 18, wherein the pre-FFT processing device includes a cyclic prefix remover.

22. The apparatus of claim 21, wherein the adjusting device includes a timing controller for generating a control signal for controlling the operation of the cyclic prefix remover according to the timing offset.

23. An method for sampling timing compensation at a receiver of a communication system, wherein each of a first symbol and a second symbol comprising at least two pilot signals transmitted via a first and a second pilot subchannels respectively, and the first and the second pilot subchannels comprise a first and a second pilot indexes respectively, the method comprising:

processing the first and the second symbols in a time domain;

transforming the first and the second symbols to a frequency domain;

generating a frequency response of the first and the second symbols according to the pilot signals of the first and the second symbols respectively;

calculating a timing offset according to the sampling frequency offset, wherein the sampling frequency is generated according to the frequency responses of the first and the second symbols;

performing sampling timing compensation according to an phase rotation corresponding to the timing offset; and

adjusting the operation of the step of processing symbols in the time domain.